REMARKS

In the Final Office Action, the Examiner noted that claims 1-8 and 12-16 are pending in the application and that claims 1-8 and 12-16 are rejected. By this response, claims 1 and 12 are amended. In view of the above amendments and the following discussion, the Applicant submits that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 1-8 and 12-15

The Examiner rejected claims 1-8 and 12-15 as being unpatentable over Mori et al. (U.S. Patent Application Publication No.: 2002/0088977 A1, published July 11, 2002). The rejection is respectfully traversed.

More specifically, the Examiner stated that Mori discloses, with reference to FIG. 11, an integrated circuit die (57) having an array of micro-bumps (58) disposed in a first pattern; an integrated circuit package (64) having an array of landing pads disposed on an inside surface in a second pattern; and an interposing structure (62) disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the package. (Final Office Action, pp. 2-3). The Examiner conceded that Mori does not disclose that the interposer couples a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite the first position and to a second landing pad in the array of landing pads. (Final Office Action, p. 3). The Examiner stated, however, that an interposer shown in FIG. 1B of Mori includes a first micro-bump coupled to first and second landing pads. (Final Office Action, p. 3). The Examiner concluded that it would have been obvious to use the interposer shown in FIG. 1B to modify the structure in FIG. 11 for the purpose of providing a single input signal to several output signals. (Final Office Action, p. 5). The Applicant respectfully disagrees.

In FIG. 11 of Mori, the interposer (62) is provided between a printed circuit board (64) and an integrated circuit die (57). In Applicant's invention, however, the interposing structure is disposed "inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package." (Applicant's claim 1; see also Applicant's FIG. 10). Coupling an interposer to a printed circuit board, as disclosed by Mori, does not teach or suggest an interposing structure disposed inside an integrated circuit package. The interposer (62) of Mori is disposed on top of the printed circuit board, rather than inside the printed circuit board or any other package.

In the interests of furthering prosecution, the Applicant has amended claim 1 to recite "an array of solder balls disposed on an outside surface of the integrated circuit package." The printed circuit board of Mori is not an integrated circuit package and does not include an array of solder balls disposed on an outside surface thereof. Therefore, Mori does not teach, suggest, or otherwise render obvious Applicant's invention recited in claim 1. Namely, Mori does not teach or suggest an interposing structure dispose inside an integrated circuit package having an array of landing pads disposed on an inside surface and an array of solder balls disposed on an outside surface.

Independent claim 12 recites features similar to those in claim 1 emphasized above. Namely, claim 12 recites, among other features, a means for coupling disposed inside an integrated circuit package, where the integrated circuit package includes an array of landing pads disposed on an inside surface and an array of solder balls disposed on an outside surface. For the same reasons set forth above, the Applicant contends that Mori does not teach or suggest the invention of Applicant's claim 12.

Finally, claims 2-8 and 13-15 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Mori does not render obvious Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 13-15 are also nonobvious and are allowable. Therefore, the Applicant contends that claims 1-8 and 12-15 are patentable over Mori and, as such, fully satisfy the requirements of

35 U.S.C. §103. The Applicant respectfully requests that the rejection of such claims be withdrawn.

B. Claim 16

The Examiner rejected claim 16 as being unpatentable over Mori in view of Berlin (U.S. Patent 6,104,082, issued August 15, 2000). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Mori does not disclose the integrated circuit die being an application specific integrated circuit (ASIC). (Final Office Action, p. 7). The Examiner stated, however, that Berlin teaches an ASIC integrated circuit die. (Final Office Action, p. 8). The Examiner concluded that it would have been obvious to use the ASIC of Berlin in the structure of Mori. (Final Office Action, p. 8). The Applicant respectfully disagrees.

Claim 16 depends from claim 12 and recites additional features therefor. Berlin, as shown in FIG. 2, discloses an interposer (60') disposed between a plurality of chips and a substrate (68). The interposer of Berlin is not disposed inside the substrate, and the substrate does not include an array of solder balls on an outside surface thereof. Berlin does not teach, suggest, or otherwise render obvious a coupling means disposed inside an integrated circuit package having an array of landing pads disposed on an inside surface and an array of solder balls disposed on an outside surface, as recited in Applicant's claim 12. As described above, Mori also fails to teach or suggest such a feature. Since neither Mori nor Berlin teach or suggest Applicant's invention, no conceivable combination of the cited references renders obvious Applicant's invention. Thus, the Applicant contends that the claim 16, which depends from claim 12, is patentable over the cited references and, as such, fully satisfies the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly,

both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 14, 2006.

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